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SEMICONDUCTOR DEVICE WITH PERIPHERAL BREAKDOWN PROTECTION

FIELD OF INVENTION

The present embodiments relate to semiconductor devices.

BACKGROUND

Integrated circuits (ICs) and other electronic devices often include arrangements of interconnected field effect transistors (FETs), also called metal-oxide-semiconductor field effect transistors (MOSFETs), or simply MOS transistors or devices. A typical MOS transistor includes a gate electrode as a control electrode, and spaced apart source and drain electrodes. A control voltage applied to the gate electrode controls the flow of current through a controllable conductive channel between the source and drain electrodes.

Power transistor devices are designed to be tolerant of the high currents and voltages that are present in power applications such as motion control, air bag deployment, and automotive fuel injector drivers. One type of power MOS transistor is a laterally diffused metal-oxide-semiconductor (LDMOS) transistor. In an LDMOS device, a drift space is provided between the channel region and the drain region.

LDMOS devices are often used in applications, such as automotive applications, involving operational voltages greater than 40 volts. Various features of the LDMOS devices are designed to increase the voltage at which device breakdown (e.g., avalanche breakdown) occurs. For example, breakdown is often prevented through a reduced surface field (RESURF) structure in the LDMOS device design. The RESURF structure is designed to deplete the drift space of the LDMOS device in both vertical and lateral directions, thereby reducing the electric field either near the edge of, or inside, the drift region and thus raising the off-state breakdown voltage (BV_{dss}) of the device. Unfortunately, RESURF structures only address breakdown in areas near or inside the drift region. The breakdown voltage of the device may be established by breakdown that occurs in other locations.

BRIEF DESCRIPTION OF THE DRAWINGS

The components and the figures are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the various embodiments. Moreover, in the figures, like reference numerals designate corresponding parts throughout the different views.

FIG. 1 is a cross-sectional, schematic, partial view of an exemplary LDMOS transistor with internal and peripheral breakdown protection in accordance with one embodiment.

FIG. 2 is a cross-sectional, schematic, partial view of an exemplary LDMOS transistor with peripheral breakdown protection in accordance with one embodiment.

FIG. 3 is a flow diagram of an exemplary fabrication sequence to construct an LDMOS transistor peripheral breakdown protection in accordance with one embodiment.

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

Embodiments of laterally diffused metal oxide semiconductor (LDMOS) and other semiconductor devices and electronic apparatus with breakdown protection are described. The breakdown protection is provided by a break-

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down protection region disposed between a device isolation region and a body region or other region of the semiconductor device through which charge carriers pass during operation. The breakdown protection may be provided along a lateral periphery of the device. The breakdown protection region may be configured as a peripheral breakdown protection region or ring.

The breakdown protection may be useful in semiconductor devices having one or more features directed to achieving a high breakdown voltage level. For example, the semiconductor devices may include a semiconductor-on-insulator (SOI) substrate, a RESURF arrangement, and/or a diminished drift region at or near the drain (e.g., an open drain arrangement), as described herein. These and/or other aspects of the semiconductor devices may be used or provided to increase the off-state breakdown voltage (e.g., BV_{dss}) and thereby increase the voltage rating of the semiconductor device.

Power transistors (e.g., LDMOS transistor devices) with a high breakdown voltage level may be useful in power switch regulators for automotive, consumer, and other applications. For example, a field drift LDMOS transistor device with high side capability (e.g., an operational condition in which all source/body and drain terminals are higher than ground) may be useful as a high voltage power switch. In order to prevent breakdown caused by voltage overshooting during switching or electrostatic discharge (ESD) events, a power LDMOS device may be configured to have a breakdown voltage level at least 30-40 Volts higher than the operational voltage, which may be above 100 Volts. The breakdown voltage level (e.g., BV_{dss}) may thus be determinative of the voltage rating of a power transistor.

The breakdown voltage level of a power transistor may be adversely affected by potential pinning at an edge or periphery of the device. The potential may be pinned, or fixed, through charge inversion at or along a wall of a device isolation region, such as a deep trench isolation (DTI) region. For example, the potential pinning and resulting degradation of the breakdown voltage level may occur in p-channel LDMOS transistor devices configured for high voltage operation (e.g., above 100 Volts) with a semiconductor-on-insulator (SOI) substrate. The edge degradation occurs as the source/body voltage near the DTI region is biased higher (e.g., above 100 Volts). Eventually, charge inversion may occur in the n-type body well region disposed at or along the device isolation region walls (e.g., the SOI and/or DTI walls). Once the inversion occurs, the potential at that location is fixed, or pinned. When inversion pinning occurs at either the SOI and/or DTI walls, the pinning potential may be about 15-30 Volts lower than the source/body voltage depending on the thickness (e.g., oxide thickness) of the SOI and DTI walls. For example, with a source/body bias of 110V, the pinning potential may be between about 80-95 Volts, which may be too high for safe device operation and may cause reliability issues. Such high potential pinning at the isolation walls may generate multiple areas under high electric field stress, which may be referred to as hot spots for impact ionization and lead to early avalanche breakdown. One hot spot is located at an upper corner of the DTI region (e.g., at the interface between the DTI and STI regions). Another hot spot is located between the drain region and the insulator layer of the SOI substrate. The inversion and potential pinning may thus lead to breakdown voltage (e.g., BV_{DSS}) degradation in SOI-based p-channel LDMOS transistor devices.

The breakdown protection region of the semiconductor devices may be provided to prevent the potential pinning